ABSTRACT

A microsystem-on-a-chip comprises a bottom wafer of normal thickness and a series of thinned wafers can be stacked on the bottom wafer, glued and electrically interconnected. The interconnection layer comprises a compliant dielectric material, an interconnect structure, and can include embedded passives. The stacked wafer technology provides a heterogeneously integrated, ultra-miniaturized, higher performing, robust and cost-effective microsystem package. The highly integrated microsystem package, comprising electronics, sensors, optics, and MEMS, can be miniaturized both in volume and footprint to the size of a bottle-cap or less.